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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/654,884	09/05/2003	Chie Kabuo	56937-087	6627
7590 01/26/2006				
McDERMOTT, WILL & EMERY 600 13th Street, N.W. Washington, DC 20005-3096		EXAMINER LEVIN, NAUM B		
		ART UNIT 2825 PAPER NUMBER		

DATE MAILED: 01/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

HFD

Office Action Summary	Application No. 10/654,884	Applicant(s) KABUO, CHIE	
	Examiner Naum B. Levin	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 November 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2 and 4-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2 and 4 is/are allowed.
- 6) ☒ Claim(s) 5 and 6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to application 10/654,884, and Amendment filed on 11/22/2005. The Applicant has amended claim 5 and added a new claim 6. Claims 2 and 4-6 remain pending in the application. The Examiner finds Applicant's comments persuasive on the application of Sano on the claims. However, the Examiner has found another reference, which reads on the claims as presently written.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 5 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Dangelo et al. (U.S. Patent 5,555,201).

As to claims 5 and 6 Dangelo recites:

(5) A system for estimating the performance of an integrated circuit (The process of designing an electronic circuit on a typical ECAD system ... by viewing the simulation results, the user may then determine if the represented circuit will perform correctly when it is constructed-col.5, ll.19-38), in which the performance of an integrated circuit is estimated based on a net list of a gate level (performance characteristics and timing parameters for a particular object in a design ... varies with the abstraction level... the performance of a circuit may be determined by simulation tools. Propagation delays through gates and other standard cells may be obtained from the component database

1712. Additional timing information is available for flip-flops and latches-col.42, ll.28-44) including a signal having correspondence to a logic description (The user interface 2401 ... indicate the common signals in multiple representations currently on the screen-col.46, ll.40-51) of a register transfer level (the designer re-formulates the design as a register-transfer level (RTL) description of the circuit in terms of pre-designed functional blocks, such as memories and registers –col.16, ll.3-6, col.16, ll.31-49), comprising:

display means (Fig. 16, pos. 1606; Fig. 24, pos. 2401, 1606) for displaying a reach delay time of each of signals, which reaches a partial circuit on a net list of a gate level (Figs. 18-19; col.19, ll.11-15) corresponding to a specified portion on the logic description (The timing information of an object may be displayed as a waveform. Margin (slack) information refers to delays introduced into the circuit to ensure that signals arrive at various locations in a circuit at the appropriate times –col.43, ll.51-55) (col.11, ll.61-67; col.12, ll.54-67; col.17, ll.6-13; col.19, ll.11-15; col.43, ll.43-67; col.44, ll.24-27).

(6) A system for estimating the performance of an integrated circuit (The process of designing an electronic circuit on a typical ECAD system ... by viewing the simulation results, the user may then determine if the represented circuit will perform correctly when it is constructed-col.5, ll.19-38), in which the performance of an integrated circuit is estimated based on a net list of a gate level (performance characteristics and timing parameters for a particular object in a design ... varies with the abstraction level... the performance of a circuit may be determined by simulation tools. Propagation delays through gates and other standard cells may be obtained from the component database

1712. Additional timing information is available for flip-flops and latches—col.42, ll.28-44) including information referred by a logic description (the logic description of a design is written onto a programmable hardware device, e.g., an PROM or a gate array. This emulated form of the device is then available for other users to use in systems for which the device is being designed, e.g., software developers —col.44, ll.1-23) of a register transfer level (the designer re-formulates the design as a register-transfer level (RTL) description of the circuit in terms of pre-designed functional blocks, such as memories and registers —col.16, ll.3-5, col.16, ll.31-49), comprising:

display means (Fig. 16, pos. 1606; Fig. 24, pos. 2401, 1606) for displaying a reach delay time of each of signals, which reaches a partial circuit on a net list of a gate level (Figs. 18-19; col.19, ll.11-15) corresponding to a specified portion on the logic description (The timing information of an object may be displayed as a waveform. Margin (slack) information refers to delays introduced into the circuit to ensure that signals arrive at various locations in a circuit at the appropriate times —col.43, ll.51-55) (col.11, ll.61-67; col.12, ll.54-67; col.17, ll.6-13; col.19, ll.11-15; col.43, ll.43-67; col.44, ll.24-27).

Allowable Subject Matter

4. Claims 2 and 4 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest or render obvious:

A system for estimating the performance of an integrated circuit, in which the performance of an integrated circuit is estimated based on a net list of a gate level including a signal having correspondence to a logic description of a register transfer level, comprising floorplan means for arranging a device model inside of the net list of the gate level within a specified region; invariable part optimizing means for inserting a buffer to satisfy a design rule with respect to the signal having the correspondence to the logic description, and performance calculating means for calculating the performance of the net list of the gate level by the use of an interconnection prediction value by the interconnection predicting means.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2825

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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VUTHE SIEK
PRIMARY EXAMINER